CLAIMS:

1. A network device comprising:

at least one network port;

a clock generating a timing signal;

address resolution logic (ARL) tables configured to store and maintain network address data; and

address resolution logic coupled to said ARL tables and said clock, and configured to search said ARL tables and to perform updates and inserts to said ARL tables based on a learning function, said searching and said updates and inserts being performed concurrently during alternating slots of said timing signal;

wherein said address resolution logic is configured to search said ARL tables for a destination address based on a data packet received at a port of said at least one port, and when said search returns a destination address, said address resolution logic is configured to update a related record of said ARL tables based on said learning function.

2. The network device of claim 1, wherein said address resolution logic is configured to perform multiple searches of said ARL tables and to perform said updates and inserts concurrently during alternating slots of said timing signal, and to perform said updates and inserts based at least one result of said multiple searches.

3. The network device of claim 1, wherein said address resolution logic is configured to utilize a data read related to learning updates for searches, when a search and an update attempt to read a same record in a same cycle.

4. The network device of claim 1, wherein said network device is configured to block updates and inserts associated with said learning function for one search cycle of said timing signal when a search finds a destination address.

5. The network device of claim 1, wherein said address resolution logic is configured to insert records into said ARL table based on said learning function, to perform a bubble sort when inserting a record into said ARL tables, to snoop updates caused by said bubble sort, and to block any updates to records within one search step of a search being executed.

6. The network device of claim 5, wherein said searches are binary searches.

7. The network device of claim 5, wherein said address resolution logic is configured to block updates caused by said bubble sort for one search cycle of said timing signal when a search finds a destination address.

8. The network device of claim 1, wherein said address resolution logic is configured to block updates by changing a data write associated with an update being blocked to a data read for one cycle of said timing signal.

9. The network device of claim 7, wherein said address resolution logic is configured to block updates by changing a data write associated with an update being blocked to a data read for one cycle of said timing signal.

10. A network device comprising:

at least one network port;

a clock means for generating a timing signal;

address resolution logic (ARL) table means for storing and maintaining network address data; and

address resolution logic means for coupling to said ARL tables and said clock, and for searching said ARL tables and perform updates and inserts to said ARL tables based on a learning function, said searching and said updates and inserts being performed concurrently during alternating slots of said timing signal;

wherein said address resolution logic means is configured to search said ARL table means for a destination address based on a data packet received at a port of said at least one port, and when said search returns a destination address, said address resolution logic means is configured to update a related record of said ARL table means based on said learning

function.

11. The network device of claim 10, wherein said address resolution logic means is configured to perform multiple searches in said ARL table means and to perform said updates and inserts concurrently during alternating slots of said timing signal, and to perform said updates and inserts based at least one result of said multiple searches.

12. The network device of claim 10, wherein said address resolution logic means is configured to utilize a data read related to learning updates for searches, when a search and an update attempt to read a same record in a same cycle.

13. The network device of claim 10, wherein said address resolution logic means is configured to block updates and inserts associated with said learning function for one search cycle of said timing signal when a search finds a destination address.

14. The network device of claim 10, wherein said address resolution logic means is configured to insert records into said ARL table means during learning, to perform a bubble sort when inserting a record into said ARL table means, to snoop updates caused by said bubble sort, and to block any updates to records within said ARL table means within one search step of a

search being executed.

15. The network device of claim 14, wherein said searches comprise binary searches.

16. The network device of claim 14, wherein said address resolution logic means is configured to block updates caused by said bubble sort for one search cycle of said timing signal when a search finds a matching destination address for said data packet.

17. The network device of claim 10, wherein said address resolution logic means is configured to block updates by changing a data write associated with an update being blocked to a data read for one cycle of said timing signal.

18. The network device of claim 16, wherein said address resolution logic means is configured to block updates by changing a data write associated with an update being blocked to a data read for one cycle of said timing signal.

19. A method for performing searching and learning concurrently within a network device, said method comprising the steps of:

providing a network device comprising at least one port, ARL tables

configured to store and maintain data related to port addresses of said network device, and address resolution logic configured to update and insert data into said ARL tables based on a learning function;

receiving a timing signal;

receiving a data packet at a port of said at least one port;

initiating a search in said ARL tables based on said packet; and

performing said search concurrently with and updates to said ARL tables related to said learning function, said searches and updates being performed during alternating slots of said timing signal.

20. The method of claim 19, wherein

said receiving step comprising receiving a plurality of data packets at a plurality of ports of said at least one port, and

said initiating step comprises initiating a plurality of searches in parallel based on said plurality of data packets.

21. The method of claim 19, further comprising a steps of:

determining if a data read related to a search hits the same record as a data read related to a learning update, and

utilize the data read related to the learning update for said search.

22. The method of claim 15, further comprising a step of:

blocking said updates for one search cycle of said timing signal after

any search makes a match.

23. The method of claim 21, wherein said utilizing step comprises discarding any data read by said data read related to a search.

24. The method of claim 22, wherein said address resolution logic means is configured to perform a bubble sort when inserting a record into said address storage means, and said initiating a search step includes initiating a plurality of searches, and said blocking step comprises blocking updates related to said bubble sort for one search cycle of said timing signal after any search makes a match.

25. The method of claim 22, wherein said blocking step comprises changing a write related to an update into a read for one cycle of said timing signal.

26. The method of claim 24, wherein said blocking step comprises changing a write related to an update into a read for one cycle of said timing signal.